Refine Search

09/843,419

Search Results -

Terms	Documents
L6 and (fluorine or fluorinated) and (signal adj line) and (power adj line) and (via or plug)	1

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Search History

DATE: Saturday, February 07, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	<u>Set</u> <u>Name</u> result set
DB=U	SPT; PLUR=YES; OP=ADJ		
<u>L7</u>	L6 and (fluorine or fluorinated) and (signal adj line) and (power adj line) and (via or plug)	1	<u>L7</u>
<u>L6</u>	L1 and damascene	17	<u>L6</u>
<u>L5</u>	L1 and (signal adj line) and (via or plug) and (power adj line)	2	<u>L5</u>
<u>L4</u>	L1 and (fluorinated)	6	<u>L4</u>
<u>L3</u>	L1 and (fluorinated near2 oxide)	0	<u>L3</u>
<u>L2</u>	L1 and (fluorinated near (silicon adj oxide))	. 0	<u>L2</u>
<u>L1</u>	fifth near dielectric	297	<u>L1</u>

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Search Results - Record(s) 1 through 1 of 1 returned.

1. Document ID: US 6225207 B1

L7: Entry 1 of 1

File: USPT

May 1, 2001

US-PAT-NO: 6225207

DOCUMENT-IDENTIFIER: US 6225207 B1

TITLE: Techniques for triple and quadruple damascene fabrication

Full	tle Citation Front Review Classification Date Reference	Claims KWC Draw C
Clear	Generate Collection Print Fwd Refs Bkwd Refs	Generate OACS
	Terms	Documents
	L6 and (fluorine or fluorinated) and (signal adj line) and (power adj line) and (via or plug)	1

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L7: Entry 1 of 1

File: USPT

May 1, 2001

US-PAT-NO: 6225207

DOCUMENT-IDENTIFIER: US 6225207 B1

TITLE: Techniques for triple and quadruple damascene fabrication

DATE-ISSUED: May 1, 2001

INVENTOR-INFORMATION:

NAME

CITY

STATE

ZIP CODE

COUNTRY

Parikh; Suketu A.

San Jose

CA

US-CL-CURRENT: 438/622; 257/E21.579, 438/637, 438/638, 438/666, 438/700, 438/738,

438/740

TW .	\blacksquare	•		4
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Generate OACS

Search Results - Record(s) 1 through 2 of 2 returned.

1. Document ID: US 6657130 B2

L5: Entry 1 of 2

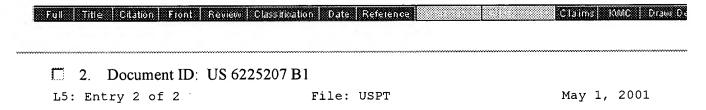
File: USPT

Dec 2, 2003

US-PAT-NO: 6657130

DOCUMENT-IDENTIFIER: US 6657130 B2

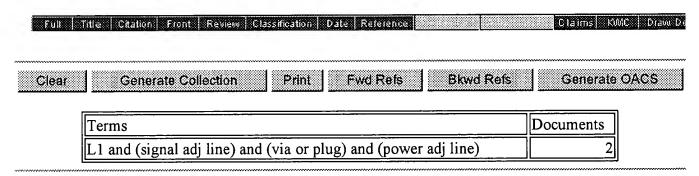
TITLE: Electrical and physical design integration method and apparatus for providing interconnections on first level ceramic chip carrier packages



US-PAT-NO: 6225207

DOCUMENT-IDENTIFIER: US 6225207 B1

TITLE: Techniques for triple and quadruple damascene fabrication



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Search Results - Record(s) 1 through 6 of 6 returned.

1. Document ID: US 6593225 B1

L4: Entry 1 of 6

File: USPT

Jul 15, 2003

US-PAT-NO: 6593225

DOCUMENT-IDENTIFIER: US 6593225 B1

TITLE: Method of forming a stacked dielectric layer on a semiconductor substrate

having metal patterns

Full Title Citation Front Review Classification Date Reference Claims RMC Draw D.

1. 2. Document ID: US 6583069 B1

L4: Entry 2 of 6 File: USPT Jun 24, 2003

US-PAT-NO: 6583069

DOCUMENT-IDENTIFIER: US 6583069 B1

TITLE: Method of silicon oxide and silicon glass films deposition

Full Title Citation Front Review Classification Date Reference Claims FMC Craw De

File: USPT

US-PAT-NO: 6500771

L4: Entry 3 of 6

DOCUMENT-IDENTIFIER: US 6500771 B1

TITLE: Method of high-density plasma boron-containing silicate glass film

deposition

Full Title Citation Front Review Classification Date Reference Claims KWC Draw De

L4: Entry 4 of 6

File: USPT

Mar 12, 2002

Dec 31, 2002

US-PAT-NO: 6355581

DOCUMENT-IDENTIFIER: US 6355581 B1

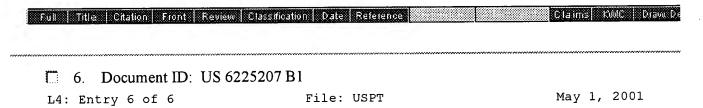
TITLE: Gas-phase additives for an enhancement of lateral etch component during high density plasma film deposition to improve film gap-fill capability

Full Title Citation Front Review	Classification Date Reference	Claims RWC Draw Do
5. Document ID: US 62	74202 D1	
3 3. Document ID. US 02	/4293 D1	
L4: Entry 5 of 6	File: USPT	Aug 14, 2001

US-PAT-NO: 6274293

DOCUMENT-IDENTIFIER: US 6274293 B1

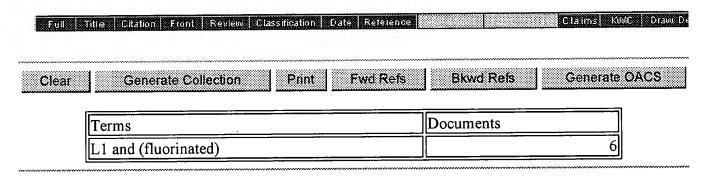
TITLE: Method of manufacturing flexible metallic photonic band gap structures, and structures resulting therefrom



US-PAT-NO: 6225207

DOCUMENT-IDENTIFIER: US 6225207 B1

TITLE: Techniques for triple and quadruple damascene fabrication



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Search Results - Record(s) 1 through 1 of 1 returned.

1. Document ID: US 6541336 B1

L9: Entry 1 of 1

File: USPT

Apr 1, 2003

US-PAT-NO: 6541336

DOCUMENT-IDENTIFIER: US 6541336 B1

TITLE: Method of fabricating a bipolar transistor having a realigned emitter

Full Title Citation Front Review Classification Date	Reference Claims NVIC Draw
Clear Generate Collection Print Fi	wd Refs Bkwd Refs Generate OACS
Terms	Documents
L8 and (cap adj layer)	

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13		

L9: Entry 1 of 1

Apr 1, 2003 File: USPT

DOCUMENT-IDENTIFIER: US 6541336 B1

TITLE: Method of fabricating a bipolar transistor having a realigned emitter

Detailed Description Text (5):

In realigned emitter devices, emitter layer 45 is generally formed by a doped chemical vapor (CVD) process. Single crystal (or epitaxial) silicon is formed when silicon is deposited on single-crystal silicon. Polysilicon silicon is formed when silicon is deposited on a dielectric layer such as silicon oxide. An anneal step is used to drive the dopant from epitaxial region 55 into emitter 30. Because epitaxial region 55 is essentially single crystal silicon the diffusion rate of arsenic is about 10 to 100 times slower than in polysilicon regions 50. Therefore, while dopant buildup may occur at the polysilicon/dielectric interface, no such buildup occurs at the epitaxial region/emitter interface and the dopant.

Detailed Description Text (16):

In FIG. 7, a fifth dielectric layer 220 is formed over entire device 80 (see FIG. 6). An emitter contact 225 is formed in fifth dielectric layer 220 through fourth dielectric layer 215 to contact polysilicon emitter 200. A base contact. 230 is formed in fifth dielectric layer 220 through first dielectric layer 170 to contact extrinsic base portion 140 of base 205. A collector contact 235 is formed in fifth dielectric layer 220 through to contact emitter reach through 95. An interlevel dielectric layer 240 is formed over fifth dielectric layer 220 and first metal conductors 245 are formed in the interlevel dielectric layer contacting emitter contact 225, base contact 230 and collector contact 235.

Detailed Description Text (17):

In one example <u>fifth dielectric</u> layer 220 is boro-phosphorus-silicon glass (BPSG) formed by PECVDI interlevel dielectric layer 240 is tetraethoxysilane (TEOS) oxide formed by PECVD, contacts 225, 230 and 235 are formed from tungsten by well known damascene processes and first metal conductors 245 are formed from aluminum, titanium or copper by well known damascene processes. Metal silicide may be formed at the contact silicon interfaces. Fabrication of bipolar transistor 80 is essentially complete.

Detailed Description Text (22):

In step 270, first and second cap layers are formed on over the polysilicon emitter layer. In one example, the first cap layer is 100 to 140 .ANG. of plasma enhanced chemical vapor deposition (PECVD) silicon nitride and second cap layer is 1500 to 1900 .ANG. of PECVD silicon nitride.

Refine Search

Search Results -

Terms	Documents
L8 and (cap adj layer)	_ 1

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Search History

DATE: Saturday, February 07, 2004 Printable Copy Create Case

Set Name side by side	Query	<u>Hit</u> Count	Set Name result set
DB=U	SPT; PLUR=YES; OP=ADJ		
<u>L9</u>	L8 and (cap adj layer)	1	<u>L9</u>
<u>L8</u>	L6 and ((silicon adj oxide) or (silicon adj dioxide))	13	<u>L8</u>
<u>L7</u>	L6 and (fluorine or fluorinated) and (signal adj line) and (power adj line) and (via or plug)	1	<u>L7</u>
<u>L6</u>	L1 and damascene	17	<u>L6</u>
<u>L5</u>	L1 and (signal adj line) and (via or plug) and (power adj line)	2	<u>L5</u>
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<u>L2</u>	L1 and (fluorinated near (silicon adj oxide))	0	<u>L2</u>
<u>L1</u>	fifth near dielectric	297	<u>L1</u>

END OF SEARCH HISTORY